

Laboratory 3

(Due date: **011**: October 11th, **005**: October 12th, **007**: October 13th)

OBJECTIVES

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

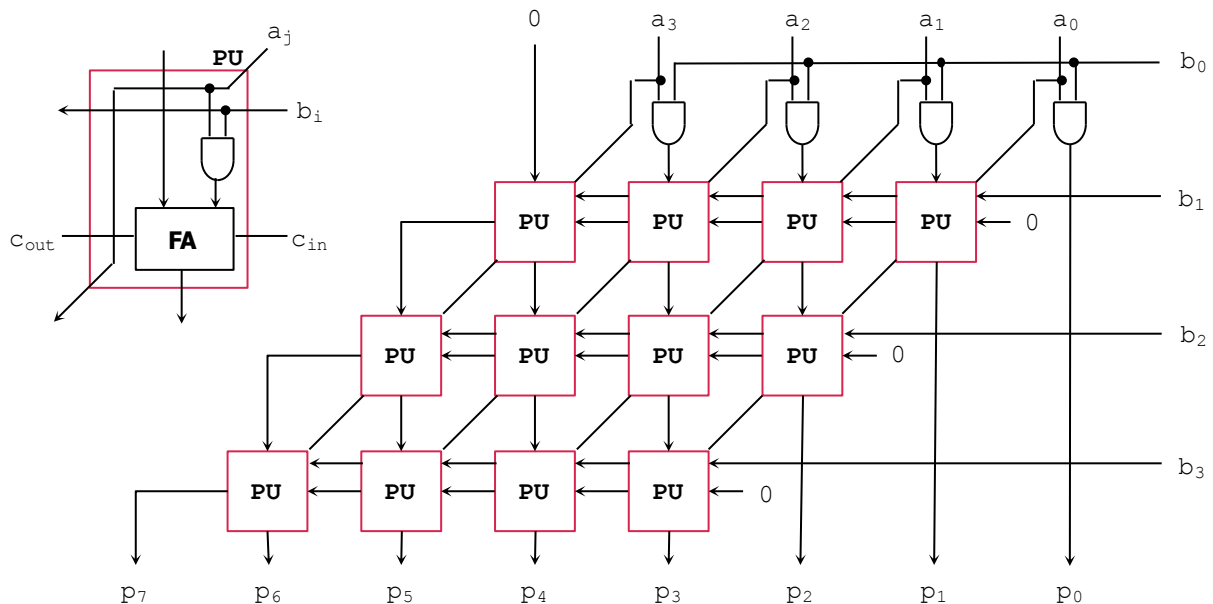
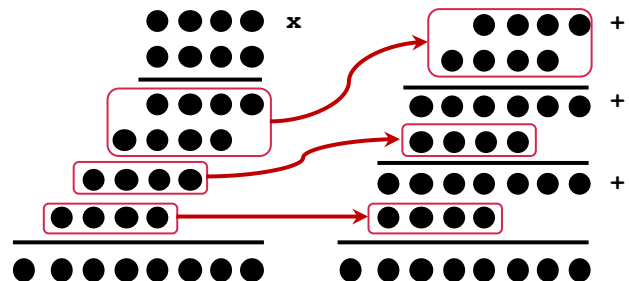
VHDL CODING

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

FIRST ACTIVITY (100/100)

DESIGN PROBLEM

- The figure depicts an array multiplier for two 4-bit unsigned numbers. It is a straightforward implementation based on adding two partial products (rows) at each stage.



PROCEDURE

- **Vivado: Complete the following steps:**
 - ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).
 - ✓ Write the VHDL code for this unsigned array multiplier. Synthesize your code.
 - Use the **Structural Description**: Create a separate .vhd file for the Full Adder, the Processing Unit (PU), and the top file (Array Multiplier).
 - ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use 'for loop'.
 - ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA.**
 - Your simulation might need more time than Vivado Simulator's default (1 us). For example, to add 5 us, you can go to the TCL console and type: `run 5 us`
 - Note that you can represent your data as unsigned integers (use Radix → Unsigned Decimal).

- ✓ I/O Assignment: Generate the XDC file associated with your board.

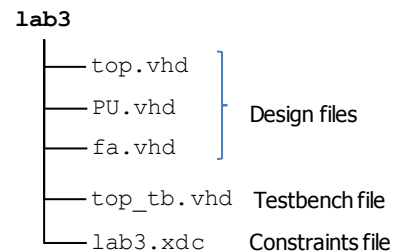
- Suggestion:

Board pin names	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀

- The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.
- ✓ Generate and download the bitstream on the FPGA and perform testing (use a sample of representative cases from your testbench). **Demonstrate this to your TA.**

SUBMISSION

- Submit to Moodle (an assignment will be created):
 - ✓ This lab sheet (as a .pdf) signed off by the TA (or instructor)
 - ✓ (As a .zip file) The five generated files: VHDL code (3 files), VHDL testbench, and XDC file. DO NOT submit the whole Vivado Project.
 - Your .zip file should only include one folder. Do not include subdirectories.
 - It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.
 - You should only submit your source files AFTER you have demoed your work. Submission of work files without demoing will be assigned NO CREDIT.



TA signature: _____

Date: _____